# DIGITAL LOGIC CIRCUITS Model: DLC-101200A

## **SPECIFICATION**

## **I. FEATURES**

- 1. THIS DEVICE INCLUDES SOME BASIC EXPERIMENT UNITS AND CAN BE EXPANDED TO THE ADVANCED SYSTEM. MODULAR DESIGN MAKES IT EASY TO USE AND MAINTAIN.
- 2. EACH EXPERIMENT UNIT CONSISTS OF SEVERAL MODULE BOARDS. ALL INPUT AND OUTPUT SIGNALS, CONTROL FLOWS AND WIRINGS ARE SHOWN ON THE MODULE BOARDS.
- 3. CIRCUIT DIAGRAMS AND/OR BLOCK DIAGRAMS, ARE SILKSCREENPRINTED ON THE MODULE BOARD.
- 4. ALL THE TEST POINTS AND CONNECTION TERMINALS ARE BROUGHT OUT ON THE FRONT FOR EASY ACCESS AND MEASUREMENT,
- 5. CONNECTION TERMINALS ARE STANDARD .16"/4MM DIAMETER JACKS.
- 6. MAIN PANEL FRAME (STAND) IS MOLDED, SPECIALLY TREATED AND PAINTED FOR LONG-LASTING.

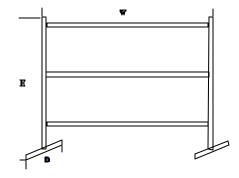
## **II. EXPERIMENTS INCLUDED:**

- 1. TTL Characteristic
- 2. CMOS Characteristic
- 3. Inverter Gate
- 4. Buffer Gate 5. AND Gate
- AND Gate
  NAND Gate
- 7 OR Gate
- 8 NOR Gate
- 9. Exclusive-OR Gate
- 10. And-Or-Inverter
- 11. Open-Collector Integrated Circuits
- 12. Three-State Gates
- 13. TTL To Cmos Interface Circuits
- 14. CMOS To TTL Interface Circuits
- 15. Pulse Conditioning Circuit
- 16. Transistor Oscillation Circuit
- 17. Non-Continue Mono-Stable Oscillation Circuit
- 18. Continuable Mono-Stable Oscillation Circuit
- 19. R-S Flip-Flop
- 20. J-K Flip-Flop
- 21. T Flip-Flop
- 22. D Flip-Flop
- 23. Sequential Logic
- 24. Left/Right Shift Register
- 25. Binary Counter
- 26. BCD Counter
- 27. Decoder
- 28. Multiplexer
- 29. Demultiplexer 30. Half Adder
- 31. Full Adder
- 32. Half Subtracter
- 33. Full Subtracter

## **III. SPECIFICATION**

#### A. MAIN PANEL FRAME

SIZE: 31"(W) x 16"(D) x 35"(H). MATERIAL: STEEL FRAME AND ALUMINUM RACK.



## **B. POWER SUPPLY**

 (1) VOLTAGE: +5V, +12V, & -12V.
 (2) CURRENT: 1A.
 (3) LOAD REGULATION: 3%+2mV.
 (4) POWER REGULATION: AC 110V+/-10%, 50/60Hz.
 (5) RIPPLE VOLTAGE: <20mVrms.</li>
 (6) Output overload protection.

#### C. SIGNAL GENERATOR

THE SIGNAL GENERATOR OUTPUT TTL AND CMOS SIGNALS SIMULTANEOUSLY ON THE SEPARATE TERMINALS.

3%+2mV

- 1. FREQUENCY
  - (1) ACCURACY: +/-0.01% at 1MHz.
  - (2) FAN OUT: 10 TTL loads.
- 2. VARIABLE FREQUENCY; 0.1~100KHz.
- 3. SWITCHES
- (1) Debounced.
- (2) FAN OUT: 10 TTL loads.
- 4. PULSE SIGNAL SWITCH
- (1) 2 sets, independently controlled.
  - (2) Q and inverse Q (~Q) outputs, pulse width > 5mS
  - (3) Debounced.
- (4) FAN OUT: 10 TTL loads.
- 5. DIGITAL MULTIMETER: 3 1/2 digits.

#### **D. DISPLAY**

- 1. LOGIC INDICATORS
  - (1) 10 LEDs.
  - (2) INPUT IMPEDANCE: >100KÙ.
- 2. DISPLAY
- (1) 7-segment LEDs.
  - (2) Latch, BCD 7-segment decoder/driver, DP, RBI, RBO, and 4 independent Vcc inputs.(3) Binary input.
- E. TESTING
  - 1. LOGIC LEVEL TESTER
  - (1) For TTL and CMOS.
    - (2) Result is displayed on 7-segment LED.
      - a. Input Open: "b. Logic Low: "L". c. Logic High: "H".

- 1. EXTRUDED HERMAPHRODITIC BANANA PLUGS, STANDARD 1.6"/4mm DIAMETER.
  - 2. TOTAL 30 WIRES OF LENGTH 7.9"/.2M, 31.5"/.8M AND 59"/1.5M.

#### **B. EXPERIMENT MANUAL** ENGLISH, COPYRIGHTED IN USA.

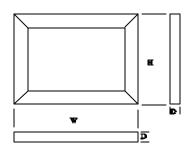
- d. Logic False: "F". e. Logic Pulse: "P".
- 2. SEQUENTIAL COMPARATOR
  - Four-trace generator; using dual-trace oscilloscope can compare 8 different sequential signals.
    For both TTL and CMOS.
    - (3) "ALT" and "CHOP" selectable.

### F. LOAD

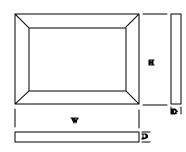
- (1) 16 LEDs display.
- (2) Red and green LEDs show the output status.
- (3) SSR and Relay: SSR; DC 3~24V input, AC 120V/3A output. Relay; DC 12V/3A.
- (4) Stepper Motor:  $1.8^{\circ}$ /step, 12VDC/0.44A.
- (5) Power Resistor: 16Ù/20W, 2 pieces. Speaker: 16Ù/20W
- (6) Lamp: two 110VAC/60W.
- (7) Sensor: photoconductive cell (cds) and phototransistor.
- (8) Keyboard: 12 keys; all keys are labeled and accessible.

### G. MODULE BOARD

- 1. USING COMBINATION OF SMALL COMPONENT AND MODULE BOARDS FOR EXPERIMENTS.
- 2. BOARD SIZE: Type-A: .80Mx1.50M, Type-B: 1.6Mx1.6M, WHITE



COLOR. Type-M: 13.4"/.34m (W) X 9.45"/.24m(H) X 1.9"/.048m (D).,



PLASTIC EXTRUSION, BLACK COLOR, 3mm THICK.

## **IV. ACCESSORIES**

## **A. CONNECTION WIRES**